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REVIEW ON CANNY EDGE DETECTION

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Abstract— Edge detection is one of the key stages in image processing .In this paper using canny edge detection algorithm, Edges will detect the efficiently with reduction in the processing speed and reduced the memory requirement. Canny edge detection algorithm reduces the latency and increase the throughput with no loss in edge detection performance and algorithm which has the ability to compute edge of multiple blocks at the same time. Canny developed an approach to derive an optimal edge detector for clean and noisy images the canny edge detection algorithm yield better edge detection result.

Keywords— Edge Detection, Optimal Edge Detector, Latency, Throughput.

I. INTRODUCTION

EDGE detection is the most common preprocessing step in many image processing algorithms such as image segmentation, image enhancement, tracking and image/video coding [3]. In digital image processing, The term edge is a collection of the pixels it refers to the part where the brightness of the image local area changes significantly in digital image processing [1]. The general methods of edge detection are first order Derivative-gradient method, Second-Order Derivative and Optimal Edge Detection to detect the edges proposed by digital image processing. A lot of edge detection algorithms, such as, Robert detector, Kirsch detector, Gauss-Laplace detector, Prewitt detector and Canny detector have been proposed. Among the existing edge detection algorithms, the Canny edge detector has remained a standard for many years and has best performance[9].

Its superior performance is due to the fact that the Canny algorithm performs hysteresis thresholding which requires computing high and low threshold based on the entire image statistics. Unfortunately, this feature makes the Canny edge detection algorithm not only more computationally complex as compared to other edge detection algorithms, such as the Roberts and sobel algorithms, but also necessitates additional pre-processing computations to be done on the entire image. As a result, a direct implementation of the canny algorithm has high latency and cannot be employed in real-time applications.

II. LITERATURE REVIEW

Qian Xu, Srenivas Varadarajan, Chaitali Chakrabarti, Fellow, IEEE, and Lina J. Karam, Fellow, IEEE "A Distributed Canny Edge Detector: Algorithmand FPGA Implementation**"** The Canny edge detector is one of the most widely used edge detection algorithms due to its superior performance. It is more intensive as compared to other edge detecting algorithms, but it also has a higher latency because it is based on frame-level statistics. In this paper, we propose a mechanism to implement the Canny algorithm at the block level without any loss in edge detection performance compared with the original frame-level Canny algorithm. Directly applying the original Canny algorithm at the block-level leads to excessive edges in smooth regions and to loss of significant edges in high-detailed regions since the original Canny computes the high and low thresholds based on the frame-level statistics. To solve this problem, we present a distributed Canny edge detection algorithm that adaptively computes the edge detection thresholds based on the block type and the local distribution of the gradients in the image block. It is capable of supporting fast edge detection of images and videos with high resolutions, including full-HD since the latency is now a function of the block size instead of the frame size [2].

Paulo Ricardo Possa, Student Member, IEEE, Sidi Ahmed Mahmoudi, Naim Harb,Carlos Valderrama, Senior Member, IEEE, and Pierre Manneback "A Multi-Resolution FPGA-Based Architecture for Real-Time Edge and Corner Detection."This work [4] presents a new flexible parameterizable architecture for image and video processing with reduced latency and memory requirements, supporting a variable input resolution. The proposed architecture is optimized for feature detection, more specifically, the canny edge detector and the Harris corner detector. The architecture contains neighborhood extractors and threshold operators that can be parameterized at runtime. A performance analysis of the FPGA and the GPU implementations, and an extra CPU reference implementation, shows the competitive throughput of the proposed architecture even at a much lower clock frequency than those of the GPU and the CPU. Maintain a reliable performance with noisy images, low latency and memory requirements [5].

In Kyu Park, Member, IEEE, Nitin Singhal, Member, IEEE, Man Hee Lee, Student Member, IEEE,Sungdae Cho, and Chris W. Kim "Design and Performance Evaluation of Image Processing Algorithms on GPUs"In this work[6],A long standing challenge in the field of image processing is that intensive computation power is required to achieve high accuracy and real-time performance. Recently, GPU has evolved into an extremely powerful computation resource. For example, NVIDIA GTX 280 with 240 processing cores at 602MHzand 1GB of GDDR3running through a 512-bit memory bus performs 933 GFLOPS in its peak performance. As a comparison, 3.2 GHz Intel Core2 Extreme (QX9775) operates at roughly 51.2 GFLOPS. The selected algorithms are parallelized efficiently on the GPU. A set of metrics was proposed to parameterize quantitatively the characteristics of parallel implementation of selected algorithms. These results can be shared and employed by other researchers to predict the appropriateness of their algorithm for parallel implementation [7].

Christos Gentsos, Calliope-Louisa Sotiropoulou and Spiridon Nikolaidis, Nikolaos Vassiliadis "Real- Time Canny Edge Detection Parallel Implementation for FPGAs" In this paper [8] Modern image processing applications demonstrate an increasing demand for computational power and memory space. Because of its algorithmic efficiency and applicability many Canny implementations have been proposed. In this novel implementation of a Canny edge detector that takes advantage of 4-pixel parallel computation. It is a pipelined architecture that uses on-chip BRAM memories to cache data between the different stages. The exploitation of both hardware parallelism and pipelining creates a very efficient design that has the same memory requirements as a design without parallelism in pixel computation. In this paper a parallel design of a real-time Canny implementation is presented. This design has been achieve a rate of 240 frames per second for 1Mpixel image on sparttan -3E occupying a 28% of the area on chip[9]

III. PROPOSED MODEL

The original canny algorithm relies on frame-level statistics to predict the high and low thresholds and thus has latency proportional to the frame size. In order to reduce the large latency and meet real-time requirements, we presented a novel distributed Canny edge detection algorithm which has the ability to compute edges of multiple blocks at the same time.

Thus our proposed project will detect the edges efficiently with reduction in the processing speed and reduced the memory. Time required to detect the edges is less**.**

IV. FUTURE WORK

Future work will be devoted to increasing the flexibility level of the architecture including a reconfigurable interconnection between the building blocks in such a way that several different processing pipelines can be created at runtime. In this way, a single architecture can be used for a wide range of image and video processing algorithms. An extension of this work will be the design of a mapping method to try to reduce the application development time. Another extension will be the addition of a histogram analysis module to automatically adjust threshold levels and/or input image equalization. Histogram analysis demands at least one pre-scan on the input image which could significantly increase the latency of the system. However, considering that in video processing the input context will not drastically change between two consecutive frames, it is possible to use the histogram analysis of one frame to adjust the architecture for the next frame, without increasing the latency.

Reference

[1] M.Rathod PG Student, ME Communication System, L.J. Institute of Engineering and Technology. "Edge Detection in VHDL"IEEE2014

[2] C. Gentsos, C. Sotiropoulou, S. Nikolaidis, and N. Vassiliadis, "Real-time canny edge detection parallel implementation for FPGAs," in Proc.IEEE ICECS, Dec. 2010, pp. 499–502

[3] Qian Xu, Srenivas Varadarajan, Chaitali Chakrabarti, Fellow, IEEE, and Lina Karam, Fellow, IEEE "A Distributed Canny Edge Detector: Algorithm and FPGA Implementation" IEEE Transactions On Image Processing, VOL. 23, NO. 7, JULY 2014

[4] R. Maini and H. Aggarwal, "Study and comparison of various image edge detection techniques,"International Journal of Image Processing (IJIP), vol. 3, no. 1, pp. 1–12, 2009.

[5] K. Park, N. Singhal, M. H. Lee, S. Cho, and C. W. Kim, "Design and performance evaluation of image processing algorithms on GPUs," IEEE Trans. Parallel Distrib. Syst., vol. 22, no. 1, pp. 91–104, Jan. 2011.

[6] N. D. Narvekar and L. J. Karam, "A no-reference image blur metric based on the cumulative probability of blur detection (CPBD)," IEEE Trans. Image Process., vol. 20, no. 9, pp. 2678–2683, Sep. 2011.

[7] Gentsos, C. Sotiropoulou, S. Nikolaidis, and N. Vassiliadis, "Real-time canny edge detection parallel implementation for FPGAs," in Proc. IEEE ICECS, Dec. 2010, pp. 499–502.

[8] H. Zeljko, V. Suzana and H. Verica, "Improved Canny Edge Detector in Ceramic Tiles Defect Detection , "IEEEIndustrialElectronics, IECON 2006 -32nd Annual Conference, pp. 3328-3331, November 2006

[9] W. He and K. Yuan, "An improved canny edge detector and its realization on FPGA," in Proc. IEEE 7th WCICA, Jun. 2008, pp. 6561–6564.IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference , pp 3328-3331, November 2006